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(54) Title of the Invention: LAMINATED DIELECTRIC DEVICE

(57) Abstract:

PURPOSE: To form an orientated film excellent in dielectric properties, at low temperatures, by making a perovskite oxide serve as an electrode.

CONSTITUTION: A (001) $ReO_3$ metal oxide conductive thin film 2 having a similar structure to that of a perovskite crystal is formed on the surface of a substrate having crystal axis orientation. A dielectric thin film of (001) perovskite oxide dielectric material is stacked on the surface of the conductive thin film. With these processes, it is possible to stack a perovskite oxide dielectric material having excellent dielectric properties and good orientation on the surface of the conductive thin film.

[Claim]

[Claim 1] A laminated dielectric device wherein a (001) $ReO_3$ metal oxide conductive thin film having a similar structure to that of a perovskite crystal is formed on the surface of a substrate having crystal axis orientation, and a dielectric thin film of (001) perovskite oxide dielectric material is stacked on the surface of the conductive thin film.

[Detailed Description of the Invention]

[0001]

[Industrial Application Field] This invention relates to a laminated dielectric device.

[0002]

[Prior Art] A dielectric device to be used in an integrated electronic circuit is required to be thin. It is important to align crystal axes of a dielectric film in order to obtain a thin film device having excellent properties. An oriented dielectric thin film forming method is often used by which the dielectric film epitaxially grown on a single crystal substrate such as MgO by sputtering or the like.

[0003] However, since many dielectric thin films require electrodes sandwiching the dielectric material, a metal layer as an electrode is interposed between a single crystal substrate and dielectric material. Therefore, orientation properties of the dielectric thin film are reduced. A high film forming temperature of 600 °C or higher is required to form an oriented dielectric film.

[0004] At the interface between metal oxide dielectric material and electrode metal, a semiconductor barrier is likely to be formed, due to oxygen defects on the dielectric material side. The influence of this interface is hard to be neglected in the case of a very thin film. In application to a memory in particular, generation of oxygen defects at the interface progresses under a high electric

field of 500 kV/cm, resulting in fatigue of a memory dielectric film.

[0005] In order to solve these problems, some proposals use conductive perovskite oxide such as BaO, 5SrO, $5MoO_3$-δ, instead of conventional electrode metal. However, composition control is not easy to form a composite metal oxide thin film, and it is difficult to form a film which is uniform in quality and stable. More over, a conductivity is lower by one to two digits than that of metal so that it is not desired to apply these proposals to a thin film capacitor.

[0006]

[Problem to be Solved by the Invention] This invention aims at forming an oriented film having excellent dielectric properties, at a low temperature, for a laminated dielectric device with electrodes of perobskite oxide.

[0007]

[Means for Solving the Problem] The invention is characterized in that a (001) $ReO_3$ metal oxide conductive thin film having a similar structure to that of a perovskite crystal is formed on the surface of a substrate having crystal axis orientation, and a dielectric thin film of (001) perovskite oxide dielectric material is stacked on the surface of the conductive thin film.

[0008]

[Function] In the present invention, $ReO_3$, $MoO_3$, $WO_3$ and the like can be used as the metal oxide of a conductive thin film. The metal of this type is cubic crystal and has a so-called $ReO_3$ crystal structure very similar to a perobskite crystal structure.

[0009] Moreover, a lattice constant a of $ReO_3$ is 3.751 and has a small misfit smaller than 10 % of a lattice constant of $SiTiO_3$, $PbTiO_3$, $BaTiO_3$ or the like to be used as perobskite oxide dielectric material. A resistivity ρ of $ReO_3$ is $1 \times 10^{-5}$

$\Omega$·cm which is near a metal resistivity.

[0010]

[Embodiment] Fig. 1 is a cross sectional view of a laminated dielectric device according to an embodiment of the present invention. Reference numeral 1 represents an oriented substrate, and reference numeral 2 represents a conductive layer of $ReO_3$ metal oxide having a structure similar to a perobskite crystal structure and formed on the surface of the substrate 1. Reference numeral 3 represents a dielectric layer of perobskite oxide dielectric material formed on the surface of the conductive layer, and reference numeral 4 represents an upper electrode formed on the surface of the dielectric layer 3.

[0011] In the laminated dielectric device of the embodiment shown in Fig. 1, the substrate 1 is made of MgO (100) single crystal, the conductive layer 2 is made of $ReO_3$, the dielectric layer 3 is made of $SrTiO_3$, and the upper electrode 4 is made of Pt. These materials were deposited by ion sputtering. Film forming conditions are shown in Table 1.

[0012]

Table 1

| Film type | Film Thickness (ppm) | Target Material | Atmospheric gas | Substrate Temperature (°C) | Vacuum degree (Torr) |
|---|---|---|---|---|---|
| Conductive film | 1500 | Re | Ar + $O_2$ | 350 | $1 \times 10^{-4}$ |
| Dielectric film | 3000 | $SrTiO_3$ | Ar + $O_2$ | 150 to 650 | $5 \times 10^{-5}$ |
| Upper electrode | 1500 | Pt | Ar | 350 | $2 \times 10^{-5}$ |

[0013] It was confirmed by x-ray diffraction that the conductive layer 2 formed under the conditions shown in Table 1 was a single $ReO_3$ layer. The dielectric layer 3 is amorphous at 150 to 250 °C, and at a higher substrate temperature, it is a single layer of a cubic crystal perobskite structure. Crystallization progresses as the temperature rises.

[0014] A characteristic curve A shown in Fig. 2 is a dielectric constant of the laminated dielectric device relative to each film forming substrate temperature. At a substrate temperature of 350 °C or higher, the (001) plane appears as shown in an x-ray diffraction pattern shown in Fig. 3 and a dielectric constant of 250 or higher is obtained corresponding to that of bulk $SrTiO_3$. Tan δ of this device was 0.5 ± 0.2 %. The same results were also obtained by using $MoO_3$ and $WO_3$ as the material of the conductive layer.

[0015] For the purposes of comparison, a laminated dielectric device was formed by forming oriented Pt at 700 °C on the surface of a MgO (100) single crystal substrate, and sequentially forming the conductive layer 2, dielectric layer 3 and upper electrode 4 on the surface of the Pt layer in the manner similar to the embodiment. A characteristic curve B of Fig. 2 shows the relation between a film forming temperature and a dielectric constant of the dielectric material. As apparent from the comparison with the characteristic curve A, the dielectric constant of the embodiment is very high.

[0016] In addition to $SrTiO_3$, the perobskite oxide dielectric material of the present invention may be at least one of Pb, Ba, La and Ca in place of Sr and at least one of Ta, Nb, Co, Mo and Zr in place of Ti.

[0017]

[Effect of the Invention] As described in detail, according to the present invention, as the conductive film, a conductive thin film of (001) $ReO_3$ metal oxide is used which has the structure similar to that of the perobskite crystal structure and good controllability and is easy to be formed. Accordingly, the advantage can be obtained which can stack a perobskite oxide dielectric material having good orientation, as a low temperature, on the surface of the conductive thin film.

[Brief Description of the Drawings]

[Fig. 1] A cross sectional view showing an embodiment of the present invention.

[Fig. 2] A drawing showing characteristic curves of a dielectric constant relative to a substrate temperature.

[Fig. 3] An x-ray diffraction pattern diagram.

[Description of Reference Numerals]

1... substrate, 2... conductive layer, 3... dielectric layer, 4... upper electrode.

FIG. 2

SUBSTRATE TEMPERATURE

FIG. 3

INTENSITY (OPTIONAL SCALE)

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Title of the Invention: JOINING STRUCTURE OF METAL ELECTRODE TO CERAMIC THIN FILM, SEMICONDUCTOR DEVICE, AND ITS MANUFACTURE

Abstract:

PURPOSE: To prevent deterioration of the ferroelectric property of a ferroelectric film, reduction in dielectric constant, in adhesion between a metal electrode and the ferroelectric thin film, etc. to be caused by heat treatment or temporal change, and to prevent occurrence of very small mechanism cracks to be caused by stresses.

CONSTITUTION: A charge storing capacitor 118 having a five-layer structure was formed on an n-type silicon substrate 101. A ferroelectric thin film 115 is put between a first conductor thin film 114 and a second conductor thin film 116 having as a main composition the same ferroelectric material as that of the thin film 115 and added with impurities. A first metal electrode 113 and a second metal electrode 117 are respectively formed on the external surfaces of the thin films 114 and 116.

[Claim]

[Claim 1] A junction structure of a ceramic thin film and a metal electrode characterized by inserting, between a ceramic film and a metal electrode, a conductive thin film having as a main composition a same ceramic material as a ceramic material of the ceramic thin film and added with impurities to impart conductivity.

[Claim 2] The junction structure of a ceramic thin film and a metal electrode according to claim 1, wherein the metal electrode is made of platinum.

[Claim 3] The junction structure of a ceramic thin film and a metal electrode according to claim 1 or 2, wherein the ceramic thin film is a ferroelectric thin film.

[Claim 4] The junction structure of a ceramic thin film and a metal electrode according to claim 1, wherein the ceramic thin film is a ferroelectric thin film of barium titanate, the metal electrode is made of platinum, and the impurities are yttrium.

[Claim 5] The junction structure of a ceramic thin film and a metal electrode according to claim 1 or 2, wherein the ceramic thin film is a high-temperature superconductivity thin film.

[Claim 6] A semiconductor device characterized by forming a charge storage capacitor having a five-layer structure on a semiconductor substrate, a ferroelectric thin film being sandwiched between first and second conductive thin film having as a main composition a same ferroelectric material as a ferroelectric material of the ferroelectric thin film and added with impurities to impart conductivity, and first and second metal electrodes being formed on the outer surfaces of the first and second conductive thin films, respectively.

[Claim 7] The semiconductor device according to claim 6, wherein the

ferroelectric thin film is made of barium titanate, the first and second metal electrodes are made of platinum, and the impurities are yttrium.

[Claim 8] A semiconductor device characterized by forming a charge storage capacitor having a four-layer structure on a semiconductor substrate, a first conductive thin film having as a main composition ferroelectric material and added with first impurities to impart p-type conductivity being bonded to a second conductive film having as a main composition a same ferroelectric material as the ferroelectric material of the first conductive film and added with second impurities to impart n-type conductivity, and first and second metal electrodes being formed on the outer surfaces of the first and second conductive thin films, respectively.

[Claim 9] The semiconductor device according to claim 8, wherein the ferroelectric thin film is made of barium titanate, the first and second metal electrodes are made of platinum, the first impurities are yttrium and the second impurities are arsenic.

[Claim 10] A semiconductor device manufacture method comprising steps of: forming a first metal electrode on a semiconductor substrate; forming a first conductive thin film by depositing ferroelectric material on the first metal electrode by sputtering and implanting impurity ions into the deposited ferroelectric material; forming a ferroelectric thin film by depositing on the first conductive thin film a same ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering; forming a second conductive thin film by depositing on the ferroelectric thin film the same ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering and implanting impurity ions into the deposited ferroelectric material; and forming a second metal electrode on the second conductive thin film.

[Claim 11] The semiconductor device manufacture method according to claim 11, wherein the ferroelectric material is made of barium titanate, the first and second metal electrodes are made of platinum, and the impurities are yttrium.

[Claim 12] A semiconductor device manufacture method comprising steps of: forming a first metal electrode on a semiconductor substrate; forming a first conductive thin film by depositing ferroelectric material on the first metal electrode by sputtering and implanting first impurity ions into the deposited ferroelectric material to impart p-type conductivity; forming a second conductive thin film by depositing a ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering and implanting second impurity ions into the deposited ferroelectric material to impart n-type conductivity; and forming a second metal electrode on the second conductive thin film.

[Claim 13] The semiconductor device manufacture method according to claim 12, wherein the ferroelectric material is made of barium titanate, the first and second metal electrodes are made of platinum, the first impurities are yttrium and the second impurities are arsenic.

[Detailed Description of the Invention]

[0001]

[Industrial Application Fields] This invention relates to a junction structure of a ceramic thin film and a metal electrode, to a semiconductor device such as in which a charge storage capacitor is formed on a semiconductor substrate, the capacitor having the structure that a ferroelectric thin film which is one type of ceramic thin films is sandwiched between metal electrodes, and to its manufacture method. A semiconductor device having a semiconductor memory using such a ferroelectric thin film can realize large capacity of a large scale

integrated (LSI) circuit.

[0002]

[Related Art] In recent years, miniaturization of each semiconductor device is promoted with high integration of LSI. Therefore, it is an important issue of semiconductor memories to realize a charge storage capacitor of small area and large capacity. Reduction in an area of a charge storage capacitor having a fixed capacitance per unit area decreases a charge storage amount per charge storage capacitor. As the charge storage amount is decreased, soft errors are likely to be caused by alpha rays. In order to make a soft error hard to produce, in the case of a dynamic RAM, the charge storage amount of about 40 or more fF is required.

[0003] The minimum storage amount Q of a charge storage capacitor is expressed by:

$$Q = S \cdot \varepsilon \cdot E = S \cdot \varepsilon \cdot V/d$$

where S is an area, εis a dielectric constant, d is a film thickness, E is an electric field intensity, and V is an operating voltage. Assuming that the operating voltage V is constant, Q can be expressed:

$$Q \propto S \cdot \varepsilon/d$$

[0004] If the area S is multiplied by k ($k < 1$) in order to reduce the area, it is necessary to multiply ε/d by 1/k to made the charge amount constant. To this end, either the film thickness d is multiplied by k or the dielectric constant ε is multiplied by 1/k. However, conventionally used dielectric materials such as $SiO_2$ and $Si_3N_4$ are hard to be made thin because a defect density becomes dense if a film is made thin.

[0005] Therefore, it is promising to multiply the dielectric constant ε by 1/k, a

semiconductor memory has been developed which uses a ferroelectric thin film having a high dielectric constant for the charge storage capacitor. In the case of dynamic RAM, the charge storage capacitor is designed to have a charge storage amount of about 40 fF or larger. A calculation equation for a charge storage amount can be expressed by:

$$Q = S \cdot \varepsilon_0 \cdot \varepsilon_r \cdot E$$

where $\varepsilon_0$ is a dielectric constant of vacuum and $\varepsilon_r$ is a relative dielectric constant. A relative dielectric constant $\varepsilon_r$ of $SiO_2$ is 3.9, whereas $\varepsilon_r$ ($BaTiO_3$) is nearly 5000 and $\varepsilon_r$ (PZT) is nearly 751 which are larger by two or three digits. Assuming the same structure, a necessary charge storage amount of about 40 fF can be obtained by using a ferroelectric thin film of $BaTiO_3$, PZT or the like even if the area S is reduced. This necessary charge storage amount is retained not only for conventional examples but also for embodiments.

[0006] As an example of a conventional semiconductor device, a conventional semiconductor memory applying a ferroelectric thin film to a charge storage capacitor is used. The conventional semiconductor memory will be described in detail hereinunder with reference to an accompanying drawing. Fig. 3 is a cross sectional view showing a conventional semiconductor device (semiconductor memory) applying a ferroelectric thin film to a charge storage capacitor. Reference numeral 301 in Fig. 3 represents an n-type single crystal silicon substrate. A p-channel switching FET 302 is formed on the surface of the n-type single crystal silicon substrate 301. An interlayer insulating film ($SiO_2$) 303 formed by CVD and an insulating film 304 [(100) magnesium oxide film (MgO film)] are formed on the n-type single crystal silicon substrate 301 having the switching FET 302. On this insulating film 304, a charge storage capacitor 316

using a ferroelectric thin film is formed.

[0007] The insulating film 304 made of the (100) magnesium oxide film (MnO film) is necessary for depositing a ferroelectric thin film 314 made of orientated barium titanate (BaTiO3). The reason is that dielectric characteristics and breakdown voltage can be improved by orientating a ferroelectric thin film such as barium titanate. The switching FET 302 is constituted of a p-type source region 305 and a p-type drain region 306 formed and electrically separated in the surface layer of the n-type single crystal silicon substrate 301 and a gate electrode 308 formed on a gate insulating film 307. Contact holes 309 and 311 are formed through the interlayer insulating film ($SiO_2$ film) 303 and insulating film (MgO film) 304 formed on the n-type single crystal silicon substrate 301, at positions corresponding to the source region 305 and drain region 306.

[0008] A source electrode 310 and a drain electrode 312 connected to the source region 305 and the drain region 306 via the contact holes 309 and 311 are formed in the interlayer insulating film ($SiO_2$ film) 303 and insulating film (MgO film) 304. The charge storage capacitor 316 is constituted of a lower metal electrode 313 made of platinum (Pt) having a thickness of 0.2 μm, the ferroelectric thin film 314 having a thickness of 10 μm, made of (100) barium titanate ($BaTiO_3$) and formed on the lower metal electrode 313, and an upper metal electrode 315 made of platinum (Pt), having a thickness of 0.2 μm and formed on the ferroelectric thin film 314.

[0009] The lower metal electrode 313 and upper metal electrode 315 were formed by depositing a platinum thin film by d.c. sputtering and pattering the thin film. The ferroelectric thin film ($BaTiO_3$ film) 314 was formed by depositing a (100) barium titanate ($BaTiO_3$) film having a thickness of 10 μm by high frequency

sputtering and pattering the film. The source electrode 310 is connected to the drain electrode 312 of the switching FET 302 via the contact hole 309 in the interlayer insulating film 303.

[0010] A LOCOS isolation region is made of an oxide film ($SiO_2$) having a thickness of 0.5 μm, and a surface protective film 318 is made of a nitride film ($Si_3N_4$) having a thickness of 1.0 μm. In the memory cell of this semiconductor device, current from the source electrode 310 can be stored in the charge storage capacitor 316 by connecting the source electrode 310 to the selection source after the gate electrode 308 of the switching FET 302 is selected.

[0011] In the following, sputtering will be described as conventional thin film forming techniques. According to the sputtering techniques, atmosphere gas of low pressure is changed to plasma by glow discharge, ions collide with target material serving as a cathode, and sputtered target particles are deposited on the substrate near an anode.

[0012] Magnetron sputtering techniques are known by which plasma of atmosphere gas generated by glow discharge is confined at a high density in a space contacting the target as an anode by using a transverse electromagnetic field and a.c. electric fields so that atoms to be deposited are sputtered at a high efficiency. A planar magnetron sputtering system generally used for a thin film deposition process is known, in which a magnet is disposed on the bottom of target material as a cathode to generate a traverse electromagnetic field and confine high density atmosphere plasma, and electrons are subjected to a cycloid motion to increase the plasma density near at the target surface.

[0013] An RF sputtering method using a $BaTiO_3$ ceramic target is generally used for forming a ferroelectric thin film or $BaTiO_3$ thin film.

[0014]

[Problems to be Solved by the Invention] However, ferroelectric characteristics are degraded, a dielectric constant lowers, tight adhesion between a metal electrode and a ferroelectric thin film is reduced, and the like, because of the following reasons. In a semiconductor device having a charge storage capacitor using the above-described ferroelectric thin film, platinum (Pt) is diffused from the lower metal electrode 313 and upper metal electrode 315 made of platinum (Pt) into the ferroelectric thin film ($BaTiO_3$) 314 due to heat treatment and temporal change, and Ba, Ti and O in the ferroelectric thin film ($BaTiO_3$) 314 are diffused toward the lower metal electrode 313 and upper metal electrode 315. There is another problem that mechanical fine cracks due to stress are likely to be formed at the interface between a metal electrode and ferroelectric material.

[0015] Ferroelectric characteristics are degraded, a dielectric constant lowers, tight adhesion between a metal electrode and a ferroelectric thin film is reduced, and the like, respectively due to diffusion of platinum (Pt) from the lower metal electrode 313 and upper metal electrode 315 made of platinum (Pt) into the ferroelectric thin film ($BaTiO_3$) 314. The reason for this is as follows. Since the ferroelectric material ($BaTiO_3$) is polycrystalline, as platinum (conductive member) invades between grain boundaries, a dielectric constant and dielectric characteristics are degraded. Although $BaTiO_3$ and Pt contacts at the electrode interface, if platinum enters grain boundaries, a mechanical strength is weakened.

[0016] Ferroelectric characteristics are degraded, a dielectric constant lowers, tight adhesion between a metal electrode and a ferroelectric thin film is reduced, and the like, respectively due to diffusion of Ba, Ti and O in the ferroelectric thin film ($BaTiO_3$) 314 toward the lower metal electrode 313 and upper metal

electrode 315. The reason for this is as follows. As Ba, Ti and O diffuse toward the lower metal electrode 313 and upper metal electrode 315, a low concentration layer, particularly a low oxygen concentration layer, is formed at the interface between the electrode and ferroelectric material. Electric field abnormality (irregularity) occurs in the low oxygen concentration layer, and fine cracks are formed when polarization / polarization reversal occurs so that dielectric characteristics and a mechanical strength are degraded.

[0017] Mechanical fine cracks are likely to be formed at the interface between the metal electrode and ferroelectric material. The reason for this is that displacement of atoms of ferroelectric material occurs during polarization / polarization reversal so that crystal boundaries become coarse. This displacement is likely to occur during polarization / polarization reversal at the interface between the metal electrode and ferroelectric material forming a high electric field. An object of this invention is to provide a junction structure of a ceramic thin film to a metal electrode, a semiconductor device and its manufacture method capable of preventing deterioration of the ferroelectric property of a ferroelectric film, reduction in dielectric constant, in adhesion between a metal electrode and the ferroelectric thin film, etc. to be caused by heat treatment or temporal change, and preventing occurrence of very small mechanism cracks to be caused by stresses.

[0018]

[Means for Solving the Problem] The junction structure of a ceramic thin film and a metal electrode recited in claim 1 is characterized by inserting, between a ceramic film and a metal electrode, a conductive thin film having as a main composition a same ceramic material as a ceramic material of the ceramic thin

film and added with impurities to impart conductivity. In the junction structure of a ceramic thin film and a metal electrode recited in claim 2, the metal electrode is made of platinum in the junction structure of a ceramic thin film and a metal electrode recited in claim 1.

[0019] In the junction structure of a ceramic thin film and a metal electrode recited in claim 3, the ceramic thin film is a ferroelectric thin film in the junction structure of a ceramic thin film and a metal electrode recited in claim 1 or 2. In the junction structure of a ceramic thin film and a metal electrode recited in claim 4, the ceramic thin film is a ferroelectric thin film of barium titanate, the metal electrode is made of platinum, and the impurities are yttrium in the junction structure of a ceramic thin film and a metal electrode recited in claim 1.

[0020] In the junction structure of a ceramic thin film and a metal electrode recited in claim 5, wherein the ceramic thin film is a high-temperature superconductivity thin film in the junction structure of a ceramic thin film and a metal electrode recited in claim 1 or 2. The semiconductor device recited in claim 6 is characterized by forming a charge storage capacitor having a five-layer structure on a semiconductor substrate, a ferroelectric thin film being sandwiched between first and second conductive thin film having as a main composition a same ferroelectric material as a ferroelectric material of the ferroelectric thin film and added with impurities to impart conductivity, and first and second metal electrodes being formed on the outer surfaces of the first and second conductive thin films, respectively.

[0021] In the semiconductor device recited in claim 7, the ferroelectric thin film is made of barium titanate, the first and second metal electrodes are made of platinum, and the impurities are yttrium in the semiconductor device recited in

claim 6. The semiconductor device recited in claim 8 is characterized by forming a charge storage capacitor having a four-layer structure on a semiconductor substrate, a first conductive thin film having as a main composition ferroelectric material and added with first impurities to impart p-type conductivity being bonded to a second conductive film having as a main composition a same ferroelectric material as the ferroelectric material of the first conductive film and added with second impurities to impart n-type conductivity, and first and second metal electrodes being formed on the outer surfaces of the first and second conductive thin films, respectively.

[0022] In the semiconductor device recited in claim 9, the ferroelectric thin film is made of barium titanate, the first and second metal electrodes are made of platinum, the first impurities are yttrium and the second impurities are arsenic in the semiconductor device recited in claim 8. The semiconductor device manufacture method recited in claim 10 comprises steps of: forming a first metal electrode on a semiconductor substrate; forming a first conductive thin film by depositing ferroelectric material on the first metal electrode by sputtering and implanting impurity ions into the deposited ferroelectric material; forming a ferroelectric thin film by depositing on the first conductive thin film a same ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering; forming a second conductive thin film by depositing on the ferroelectric thin film the same ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering and implanting impurity ions into the deposited ferroelectric material; and forming a second metal electrode on the second conductive thin film.

[0023] In the semiconductor device manufacture method recited in claim 11, the

ferroelectric material is made of barium titanate, the first and second metal electrodes are made of platinum, and the impurities are yttrium. The semiconductor device manufacture method recited in claim 12 comprises steps of: forming a first metal electrode on a semiconductor substrate; forming a first conductive thin film by depositing ferroelectric material on the first metal electrode by sputtering and implanting first impurity ions into the deposited ferroelectric material to impart p-type conductivity; forming a second conductive thin film by depositing a ferroelectric material as the ferroelectric material of the first conductive thin film by sputtering and implanting second impurity ions into the deposited ferroelectric material to impart n-type conductivity; and forming a second metal electrode on the second conductive thin film.

[0024] In the semiconductor device manufacture method recited in claim 13, the ferroelectric material is made of barium titanate, the first and second metal electrodes are made of platinum, the first impurities are yttrium and the second impurities are arsenic.

[0025]

[Function] A conventional charge storage capacitor has the structure that a ferroelectric thin film is directly sandwiched between metal electrodes. A semiconductor device of the present invention has the structure that a ferroelectric thin film is sandwiched between conductive thin films (or semiconductor thin films) having as a main composition elements constituting the ferroelectric thin film. It is therefore possible to delay diffusion of metal in the lower and upper metal electrodes directly into the ferroelectric thin film due to heat treatment and temporal changes, or diffusion of elements in the ferroelectric thin film toward the metal electrodes.

[0026] As compared to the conventional structure that metal electrodes directly contact the ferroelectric material, the ferroelectric thin film containing impurities functions as a buffer layer so that a change in electric field and a concentration of stress will not occur steeply. Since concentration of an electric field and stress is disperse, stress becomes small so that fine cracks are hard to be formed in metal electrodes and at the interface between the conductor and ferroelectric material. The reason for the delay of diffusion is as follows. If metal electrodes directly contact the ferroelectric material as in a conventional case, diffusion of electrode material into the ferroelectric layer along grain boundaries occurs and stress is generated at an interface between electrodes and ferroelectric material along during polarization and polarization reversal. According to the present invention, yttrium is doped into the ferroelectric material ($BaTiO_3$) by ion implantation or thermal diffusion to make the surface of the ferroelectric material semiconductive or conductive. It is therefore possible to realize the state that a buffer layer is substantially inserted at the interface between metal electrodes and ferroelectric material. Since cracks and diffusion of electrode material in the buffer layer of $BaTiO_3$ + Y do not influence the capacitor portion of $BaTiO_3$. Namely, it is possible to ultimately delay the diffusion of electrode material into the ferroelectric layer via the buffer layer.

[0027]

[Embodiments] Embodiments of the present invention will be described with reference to the accompanying drawings. Fig. 1 is a cross sectional view showing a semiconductor device applying a ferroelectric thin film to a charge storage capacitor. Reference numeral 101 in Fig. 1 represents an n-type single crystal silicon substrate. A p-channel switching FET 102 is formed on the

surface of the n-type single crystal silicon substrate 101. An interlayer insulating film ($SiO_2$) 103 formed by CVD and an insulating film 104 [(100) magnesium oxide film (MgO film)] are formed on the n-type single crystal silicon substrate 101 having the switching FET 102. On this insulating film 104, a charge storage capacitor 118 using a ferroelectric thin film is formed.

[0028] The switching FET 102 is constituted of a p-type source region 105 and a p-type drain region 106 formed and electrically separated in the surface layer of the n-type single crystal silicon substrate 101 and a gate electrode 108 formed on a gate insulating film 107. Contact holes 109 and 111 are formed through the interlayer insulating film ($SiO_2$ film) 103 and insulating film (MgO film) 104 formed on the n-type single crystal silicon substrate 101, at positions corresponding to the source region 105 and drain region 106. A source electrode 110 and a drain electrode 112 connected to the source region 105 and the drain region 106 via the contact holes 109 and 111 are formed in the interlayer insulating film ($SiO_2$ film) 103 and insulating film (MgO film) 104.

[0029] The charge storage capacitor 118 is constituted of five layers: a lower metal electrode 113 made of platinum (Pt), having a thickness of 0.2 μm and formed on the interlayer insulating film ($SiO_2$ film) 103 and insulating film (MgO film) 104; a first conductive thin film 114 having a thickness of 5 μm, formed on the lower metal electrode 113 and made of elements (Ba, Ti, O) constituting a ferroelectric thin film 115 of barium titanate added with impurities (yttrium: Y) at 5.0 wt.%; the ferroelectric thin film 115 and a thickness of 10 μm and made of (100) barium titanate ($BaTiO_3$); a second conductive thin film 116 having a thickness of 5 μm and made of elements (Ba, Ti, O) constituting the ferroelectric thin film 115 added with impurities (yttrium: Y) at 5.0 wt.%; and an upper metal

electrode 117 made of platinum (Pt) and having a thickness of 0.2 μm.

[0030] The lower metal electrode 113 and upper metal electrode 116 were formed by depositing a platinum thin film by d.c. sputtering and pattering the thin film. The ferroelectric thin film 114 constituting the charge storage capacitor was formed by depositing a (100) barium titanate ($BaTiO_3$) film by high frequency sputtering and pattering the film. The source electrode 110 is connected to the drain electrode 112 of the switching FET 102 via the contact hole 109 in the interlayer insulating film 103. A surface protective film 119 is made of a nitride ($Si_3N_4$) film having a thickness of 1000 nm, and a LOCOS isolation region 120 is made of an oxide film ($SiO_2$) having a thickness of 500 nm.

[0031] In the memory cell of this semiconductor device, a current signal from the source electrode 110 can be stored in the charge storage capacitor 116 by connecting the source electrode 110 to the selection source after the gate electrode 108 of the switching FET 102 is selected. According to the first embodiment of the present invention described above, disadvantages to be caused by heat treatment and temporal change of a conventional semiconductor device can be mitigated.

[0032] Namely, diffusion of platinum (Pt) from the lower metal electrode 113 and upper metal electrode 116 made of platinum (Pt) into the ferroelectric thin film ($BaTiO_3$) is delayed, and diffusion of Ba and Ti of the ferroelectric thin film ($BaTiO_3$) 114 toward the lower metal electrode 113 and upper metal electrode 116 is delayed. It is possible to mitigate that ferroelectric characteristics are degraded, a dielectric constant lowers, tight adhesion between a metal electrode and a ferroelectric thin film is reduced, and cracks are formed, respectively due to diffusion of these elements. A leak current density was able to be improved to

$10^{-6}$ A/cm$^2$, which was one hundredth of the leak current density of a conventional semiconductor device.

[0033] If the semiconductor device is used as a non-volatile memory by repetition of polarization and polarization reversal, mechanical fine cracks due to stress are hard to be formed. The number of write times through repetitive polarization and polarization reversal was able to be improved $10^9$ times from a conventional $10^7$ times. As the conductive thin film having as a main composition the same material as that of the ferroelectric thin film added with impurities is interposed between the metal electrode and ferroelectric thin film, diffusion of platinum of the metal electrode material into the ferroelectric thin film and diffusion of ferroelectric material into the metal electrode are delayed. The reason for this is as follows. With the structure of electrode / conductor added with impurities (buffer layer) / ferroelectric material, the distance between the electrode and ferroelectric material is elongated so that the electrode material takes a longer time to reach the ferroelectric layer. Diffusion of ferroelectric material into metal delayed more than the conventional diffusion because electric field concentration and stress concentration are relaxed.

[0034] As the conductive thin film having as a main composition the same material as that of the ferroelectric thin film added with impurities is interposed between the metal electrode and ferroelectric thin film, tight adhesion is not degraded. The reason for this is as follows. With the conventional structure of electrode / ferroelectric material, there is a large displacement of atoms during polarization of polarization and polarization reversal because of an abrupt change (concentration) in an electric field at the interface, stress is applied and cracks are likely to be formed. However, since the buffer layer (ferroelectric layer

added with impurities) is used, even if a high electric field is applied at the interface between the buffer layer and ferroelectric layer, a crystalline structure does not change greatly so that stress is hard to be applied (atoms are hard to be displaced).

[0035] As the conductive thin film having as a main composition the same material as that of the ferroelectric thin film added with impurities is interposed between the metal electrode and ferroelectric thin film, cracks are not formed. The reason for this is as follows. The same material is used as the main composition because the material having greatly changed crystal structures is likely to have stress at the changed area. The material used is like silicidation junction so that the interface (junction) between metal and ferroelectric material is moved toward the ferroelectric material side.

[0036] As the conductive thin film having as a main composition the same material as that of the ferroelectric thin film added with impurities is interposed between the metal electrode and ferroelectric thin film, cracks are likely to be formed. The reason for this is as follows. Ferroelectric material (in this case, polycrystalline ceramics) is made of crystal grains and boundaries. A diffusion speed is slow at the boundary, and if impurities invade, a phase not intended and controlled is formed at the boundary so that cracks are likely to be formed (this phenomenon can be observed often in sintered ceramics / electrode).

[0037] As the conductive thin film having as a main composition the same material as that of the ferroelectric thin film added with impurities is interposed between the metal electrode and ferroelectric thin film, electric field and stress concentrations can be avoided. The reason for this is as follows. Electric field and stress concentrations occur at a steep interface between different materials

of electrode and ferroelectric material. The conductive thin film / ferroelectric thin film added with metal / impurities removes a steep interface so that an electric field concentration can be avoided. The reason why the conductive thin film having the same main composition component is used is that material having a different main composition has different crystallinity so that cracks are likely to be formed at the different material interface.

[0038] Although barium titanate is used as the ferroelectric material in the embodiment, other materials may also be used such as lead zirconate titanate (PZT), strontium titanate ($SrTiO_3$) and lead titanate $PbTiO_3$. Although platinum is used as the electrode material in the embodiment, other materials may also be used such as a $Pt/TiN/BaTiO_3$ structure (TiN sandwitched between platinum and $BaTiO_3$) to prevent diffusion of electrode (platinum) into ferroelectric material, $InO_3$, $IrO_3$, indium oxide, and iridium oxide.

[0039] Although yttrium is used as the impurities to be added to ferroelectric material in the embodiment, niobium (Nb) and manganese (Mn) may be used in addition to yttrium (Y) in order to control conductivity of ferroelectric material. Although titanium is used as the ferroelectric material and yttrium is used as impurities in the embodiment, other material combinations may also be used such as a combination of $BaTiO_3$ + Y, Mn, Nb or Fe and a combination of PZT + Mn, Nb or Fe. The metal electrode used for the above-described ferroelectric material is selected experimentally so as to deterioration of electrode material.

[0040] Fig. 2 is a cross sectional view showing a semiconductor device applying a ferroelectric thin film to a charge storage capacitor according to the second embodiment of the present invention. Reference numeral 201 in Fig. 2 represents an n-type single crystal silicon substrate. A p-channel switching FET

202 is formed on the surface of the n-type single crystal silicon substrate 201. An interlayer insulating film ($SiO_2$) 203 formed by CVD and an insulating film [(100) magnesium oxide film (MgO film)] 204 are formed on the n-type single crystal silicon substrate 201 having the switching FET 202. On this insulating film 204, a charge storage capacitor 218 using a ferroelectric thin film is formed.

[0041] The switching FET 202 is constituted of a p-type source region 205 and a p-type drain region 206 formed and electrically separated in the surface layer of the n-type single crystal silicon substrate 201 and a gate electrode 208 formed on a gate insulating film 207. Contact holes 209 and 211 are formed through the interlayer insulating film ($SiO_2$ film) 203 and insulating film (MgO film) 204 formed on the n-type single crystal silicon substrate 201, at positions corresponding to the source region 205 and drain region 206. A source electrode 210 and a drain electrode 212 connected to the source region 205 and the drain region 206 via the contact holes 209 and 211 are formed in the interlayer insulating film ($SiO_2$ film) 203 and insulating film (MgO film) 204.

[0042] The charge storage capacitor 218 is constituted of four layers: a first conductive thin film 214 having a thickness of 5 μm, formed on the interlayer insulating film ($SiO_2$ film) 203 and insulating film (MgO film) 204, made of main constituent elements (e.g., Ba, Ti, O) constituting a ferroelectric thin film added with first impurities (yttrium: Y) at 5.0 wt.%; a second conductive thin film 215 having a thickness of 5 μm and made of main constituent elements (Ba, Ti, O) added with second impurities (arsenic: As) at 7.0 wt.%; an upper metal electrode 216 made of platinum (Pt) and having a thickness of 0.2 μm; and a lower metal electrode 213 made of platinum (Pt) and having a thickness of 0.2 μm.

[0043] The lower metal electrode 213 and upper metal electrode 216 were

formed by depositing a platinum thin film by d.c. sputtering and pattering the thin film. The first conductive thin film 214 and second conductive thin film 215 were formed by by high frequency sputtering deposition and pattering. The source electrode 210 is connected to the drain electrode 212 of the switching FET 202 via the contact hole 209 in the interlayer insulating film 203. A surface protective film 217 is made of a nitride ($Si_3N_4$) film having a thickness of 1000 nm, and a LOCOS isolation region 219 is made of an oxide film ($SiO_2$) having a thickness of 500 nm.

[0044] In the memory cell of this semiconductor device, a current signal from the source electrode 210 can be stored in the charge storage capacitor 218 by connecting the source electrode 210 to the selection source after the gate electrode 208 of the switching FET 202 is selected. The charge storage region of the charge storage capacitor 218 is constituted of the first conductive thin film 214 having a thickness of 5 μm and made of main constituent elements (Ba, Ti, O) constituting a ferroelectric thin film added with first impurities (yttrium: Y) at 5.0 wt.% and the second conductive thin film 215 having a thickness of 5 μm and made of main constituent elements (Ba, Ti, O) added with second impurities (arsenic: As) at 7.0 wt.%. The first conductive thin film 214 has a p-type conductivity and the second conductive thin film 215 has an n-type conductivity. A pn junction is formed at the interface between these thin films so that electric charges can be stored.

[0045] According to the second embodiment of the present invention described above, even if platinum diffuses from the upper metal electrode 216 made of platinum into the first conductive thin film 214 and second conductive thin film 215, it is possible to suppress deterioration of ferroelectricity, reduction in a

dielectric constant, lowered tight adhesion between the metal electrode and ferroelectric thin film, and generation of cracks. The leak current density was able to be improved to $10^{-6}A/cm^2$ which is one hundredth of a conventional semiconductor device.

[0046] To supplement the above-described diffusion, since a p-channel MOS transistor is used, electrons move from the upper electrode 216 toward the lower electrode. In this case, electrons collide with platinum atoms (neutral) to move the platinum atoms toward the ferroelectric material so that diffusion from the lower metal electrode 213 is not necessary to be considered. Since the first conductive thin film is a p-type and the second conductive thin film is an n-type, as the lower metal electrode 213 becomes positive, capacitor charges are stored at the interface between the first and second conductive thin films 214 and 215. Therefore, even if platinum invades into the first and second conductive thin films 214 and 215 and conductivity increases, the capacitance will not increase to the extent that platinum reaches the interface.

[0047] Although sputtering is used in the embodiments of the present invention, sol-gel or CVD may also be used. Although a ferroelectric thin film is used, ceramic material may be applied to a device using high temperature superconductive material (La-Ba-Cu-O, YBCO ($YBa_2Cu_3O_7$) and the like), suppressing reaction between metal electrode (e.g., platinum) and ceramic material and providing a thin film of good characteristics. Such devices are typically a switching element (Josephson element) of metal electrode - superconductive material - insulating material - superconductive material - metal electrode, and a combination of high temperature superconductivity and metal electrode is used as a lead wire (wiring connection) of charges.

[0048] In the embodiments, as a method of forming a ferroelectric thin film and adding impurities to elements constituting the ferroelectric thin film, a target having a different composition is used to deposit a ferroelectric thin film and a conductive thin film having different compositions. A semiconductor layer may be formed on the surface of a ferroelectric material by using ion implantation or thermal diffusion from deposited impurities. Although a flat plate type charge storage capacitor (planar type) is used in the embodiments, a stack type or trench type capacitor thin film of $SiO_2$ may also be used.

[0049] Although ion implantation is used to dope impurities, impurity ion implantation can be controlled at high precision through current control, and devices at high precision can be manufactured (improved yield).

[0050]

[Advantages of the Invention]

According to a junction structure of a ceramic thin film to a metal electrode, a semiconductor device and its manufacture method, a conductive thin film is inserted between a metal electrode and a ceramic thin film, ferroelectric thin film or high temperature superconductive thin film, the conductive thin film containing as its main composition the same material as that of the ceramic thin film, ferroelectric thin film or high temperature superconductive thin film, with impurities being added. It is therefore possible to delay diffusion of material of the metal electrode into the ceramic thin film, ferroelectric thin film or high temperature superconductive thin film, and diffusion of material of the ceramic thin film, ferroelectric thin film or high temperature superconductive thin film into the metal electrode, to be caused by heat treatment or temporal change. It is therefore possible to suppress deterioration of ferroelectricity, reduction in a

dielectric constant, lowered tight adhesion between the metal electrode and ferroelectric thin film, respectively to be caused by diffusion of the material, and generation of cracks. Practical advantages are enormous.

[Brief Description of the Drawings]

[Fig. 1] A diagram showing a semiconductor device according to the first embodiment of the present invention.

[Fig. 2] A diagram showing a semiconductor device according to the second embodiment of the present invention.

[Fig. 3] A diagram showing a conventional semiconductor device.

[Description of Reference Numerals]

101... n-type single crystal silicon substrate, 102... switching FET, 103... interlayer insulating film ($SiO_2$ film), 104... insulating film (MgO film), 105... source region, 106... drain region, 107... gate insulating film, 108... gate electrode, 109... contact hole, 110... source electrode, 111... contact hole, 112... drain electrode, 113... lower metal electrode (first), 114... first conductive thin film, 115... ferroelectric thin film, 116... second conductive thin film, 117... upper metal electrode (second), 118... charge storage capacitor, 119... surface protective film, 120... LOCOS isolation region.